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Claims:

1. An inspection system comprising:

an inspection apparatus for detecting positions and sizes of particles or pattern defects owned by an object to be inspected;

an image taking apparatus for taking images of the particles or the pattern defects as detected by the inspection apparatus; and

an analysis unit connected via a network to said inspection apparatus and said image taking apparatus wherein including:

a storage device for storing therein inspection data detected by said inspection apparatus and position information of regions being set within an LSI chip;

a calculation device for determining whether each defect is positioned in the region set within the LSI chip to be formed at the to-be-inspected object, and calculating failure probability from the size of the defects positioned in said region; and

a selection device for selecting particles or pattern defects with the calculated failure probability being greater than or equal to a given threshold.

2. An inspection system comprising:

an inspection apparatus for detecting positions and sizes of particles or pattern defects owned by an object to be inspected;

an image taking apparatus for taking images of the particles or the pattern defects as detected by the inspection apparatus;

and

an analysis unit connected via a network to said inspection apparatus and said image taking apparatus wherein including:

a storage device for storing therein inspection data detected by said inspection apparatus and position information of regions of one or more edge portions being set within an LSI chip to be formed at the to-be-inspected object; and

a selection device for selecting the particles or the pattern defects being absent at the regions of the one or more edge portions from the inspection data detected by said inspection apparatus.

3. An inspection system comprising;

an inspection apparatus for detecting positions and sizes of particles or pattern defects owned by an object to be inspected;

an image taking apparatus for taking images of the particles or the pattern defects as detected by the inspection apparatus; and

an analysis unit connected via a network to said inspection apparatus and said image taking apparatus wherein including:

a storage device for storing therein inspection data detected by said inspection apparatus and position information of one or more regions being set within an LSI chip to be formed at the to-be-inspected object; and

a selection device for selecting the particles or the pattern defects being positioned in designed regions from the inspection

data detected by said inspection apparatus.

4. The inspection system according to claim 1, wherein said regions are circuit blocks as formed within said LSI chip.

5. The inspection system according to claim 2, wherein said regions are circuit blocks as formed within said LSI chip.

6. The inspection system according to claim 3, wherein said regions are circuit blocks as formed within said LSI chip.

7. The inspection system according to claim 1, further comprising:

a simulation device for generating virtual defects at random position with respect to circuit graphics obtainable from mask layout data forming said LSI chip, and computing said failure probability from connection relationships of the circuit graphics and the defects.

8. The inspection system according to claim 1, wherein said position information of either regions of circuit blocks or edge portions is generated from the mask layout data forming said LSI chip.

9. The inspection system according to claim 2, wherein said position information of either regions of circuit blocks or edge portions is generated from the mask layout data forming said LSI chip.

10. The inspection system according to claim 3, wherein said position information of either regions of circuit blocks or edge portions is generated from the mask layout data forming said LSI

chip.

11. The inspection system according to claim 4, wherein said position information of either regions of circuit blocks or edge portions is generated from the mask layout data forming said LSI chip.

12. The inspection system according to claim 5, wherein said position information of either regions of circuit blocks or edge portions is generated from the mask layout data forming said LSI chip.

13. The inspection system according to claim 6, wherein said position information of either regions of circuit blocks or edge portions is generated from the mask layout data forming said LSI chip.

14. An inspection system comprising:

an inspection apparatus for detecting positions and sizes of particles or pattern defects owned by an object to be inspected;

an image taking apparatus for taking images of the particles or the pattern defects as detected by the inspection apparatus; and

an analysis unit connected via a network to said inspection apparatus and said image taking apparatus wherein including:

a storage device for storing therein inspection data detected by said inspection apparatus and layout information of an object to be inspected; and

a selection device for selecting particles or pattern defects

from the inspection data using the layout information.

15. The inspection system according to claim 14, wherein said layout information is position information as to a region within an LSI chip to be formed at the object to be inspected.

16. A method for manufacturing semiconductor devices comprising the steps of:

a fabrication step for forming circuit patterns on or over a wafer;

an inspection step for detecting positions and sizes of particles or pattern defects of the patterned wafer thereon said fabrication step;

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an extraction step for extracting the positions and the sizes of the particles or the pattern defects located in a region as preset within an LSI chip to be formed on the wafer;

a calculation step for calculating failure probability based on sizes of the defects in the region;

an extraction step for extracting the positions of the particles or the pattern defects with calculated failure probability being greater than or equal to a prespecified threshold;

a review step for taking images of the particles or the pattern defects extracted at the extraction step; and

a management step of the fabrication using results of the review step.

17. A method for manufacturing semiconductor devices according to claim 16, wherein said regions are circuit blocks to be formed

within said LSI chip.

18. A method for manufacturing semiconductor devices according to claim 17, wherein said LSI chip is a system LSI and said circuit blocks include memory portions and logic portions.

19. A method for manufacturing semiconductor devices comprising the steps of:

a fabrication step for forming circuit patterns on or over a wafer;

an inspection step for detecting positions and sizes of particles or pattern defects of the patterned wafer thereon the fabrication step;

an extraction step for extracting data of the particles or the pattern defects from the data of particles or the pattern defects detected at the inspection step using layout information of an LSI chip to be formed on the wafer;

a review step for taking images of the particles or the pattern defects extracted at the extraction step; and

a management step of the fabrication using results of the review step.

20. A method for manufacturing semiconductor devices according to claim 19, wherein said layout information is position information of one or more regions as designed within an LSI chip, and extracting the particles or the pattern defects located in the designated regions in said extraction step, and that images of the particles or the pattern defects are taken.